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Clearwater Forest
the Next Generation Intel®
Xeon® Processor with
Efficiency Cores
Don Soltis – Xeon Processor Architect, Intel Fellow
Stephen Robinson – Lead x86 CPU Architect, Intel Fellow

Notices & Disclaimers

Performance varies by use, configuration and other factors. Learn more on the Performance Index site.

Performance results are based on testing as of dates shown in configurations and may not reflect all publicly available updates. See backup for configuration details. No product or component can be absolutely secure.

Results have been estimated or simulated.

Your costs and results may vary.

Intel technologies may require enabled hardware, software or service activation.

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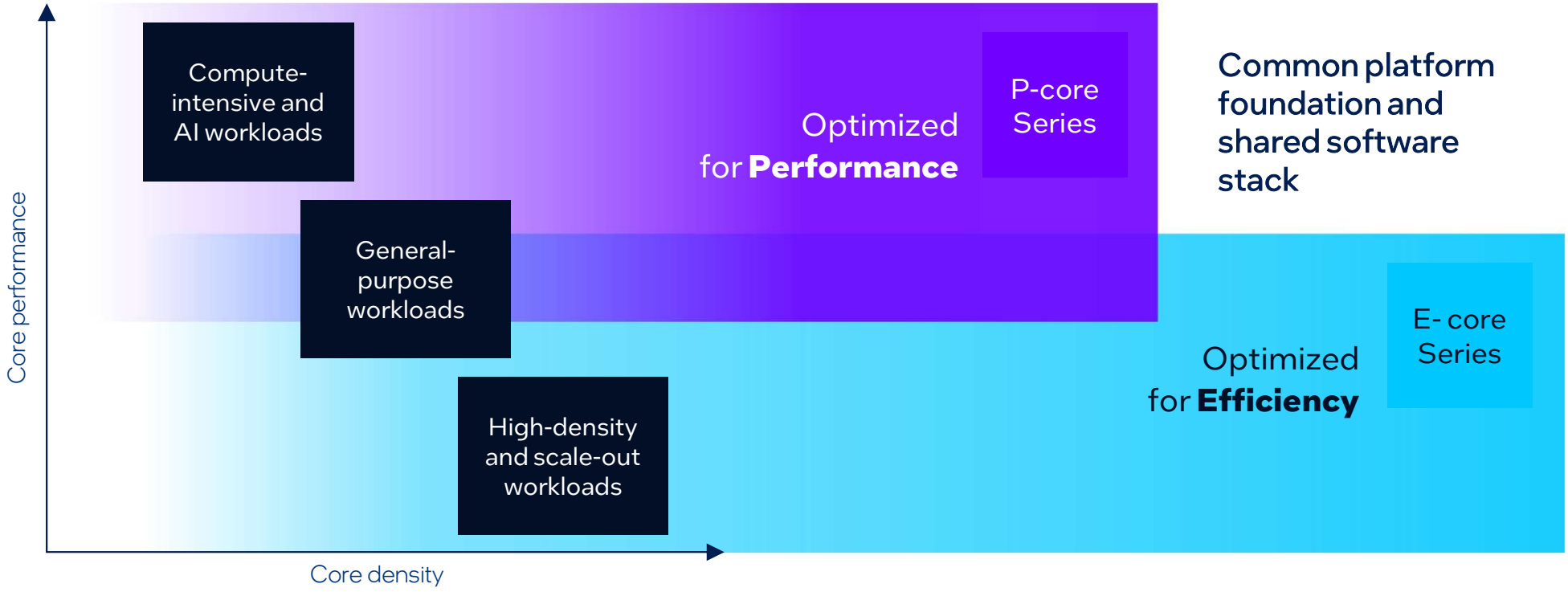
Intel® Xeon® 6, Designed to Address Market Needs

The best processors to meet diverse performance and efficiency requirements



For more Intel Xeon 6 product detail visit https://www.intel.com/content/www/us/en/content-details/834093/content-details.html

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Intel Clearwater Forest

Performance and Power Efficiency

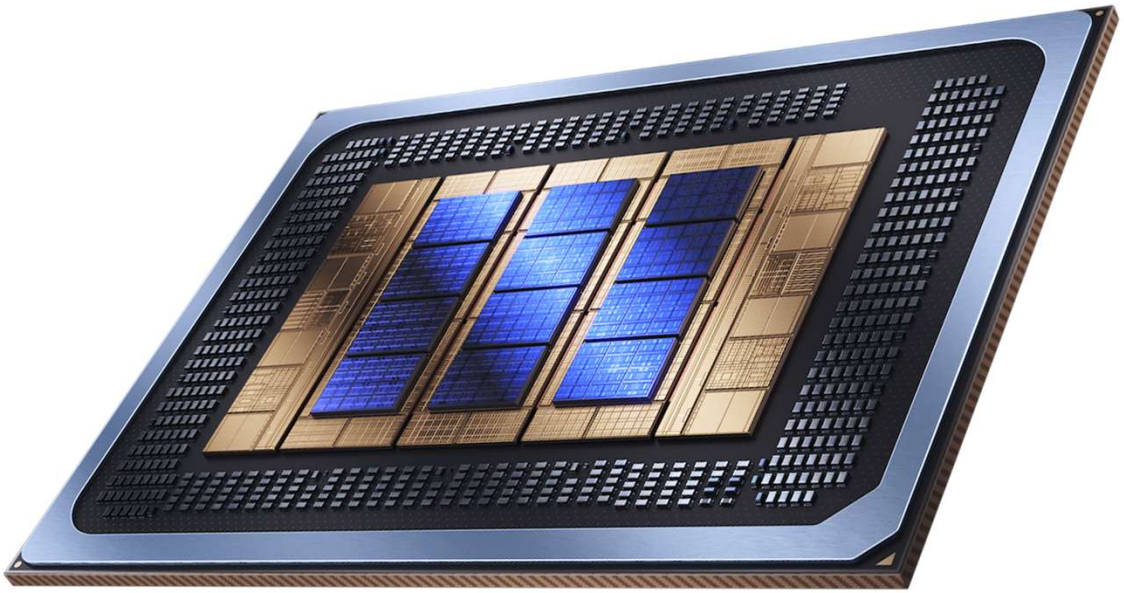
Addressing modern computing needs across data center and networking with a focus on TCO and performance per Watt for high-density compute and scale-out workloads

Intel's latest process node, 18A
Improved performance and power efficiency

Intel's latest Efficiency Core Architecture
IPC uplift tuned for 18A process

Intel Foveros Direct 3D Construction
Shorter, power efficient routes, larger last level cache (LLC)

Increased Memory Bandwidth
12 channel DDR5 8000



For more information visit https://www.intel.com/content/www/us/en/foundry/process/18a.html

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Intel 18A Process

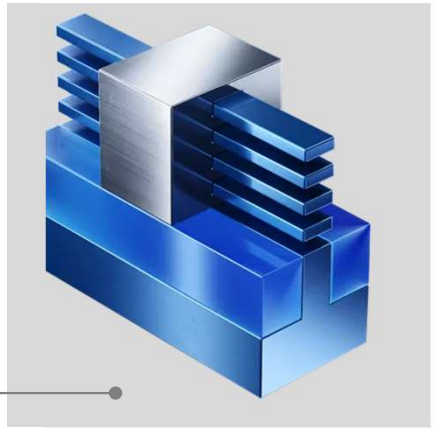
Backside metal combined with gate-all-around provide numerous benefits beyond FET Z scaling

Intel's latest process node, 18A
Lowered gate capacitance improves core logic power efficiency

Higher Cell Density
Over 90% cell utilization[1]

Improved Signal Routing
Reduces RC delay, improves power efficiency

Low Loss Power Delivery
Reduce losses by 4-5%[2]



[1] https://newsroom.intel.com/client-computing/powervia-test-shows-industry-leading-performance
[2] 2023 VLSI Symposium *"E-Core Implementation in Intel 4 with PowerVia (Backside Power) Technology"*, Manju Shamanna

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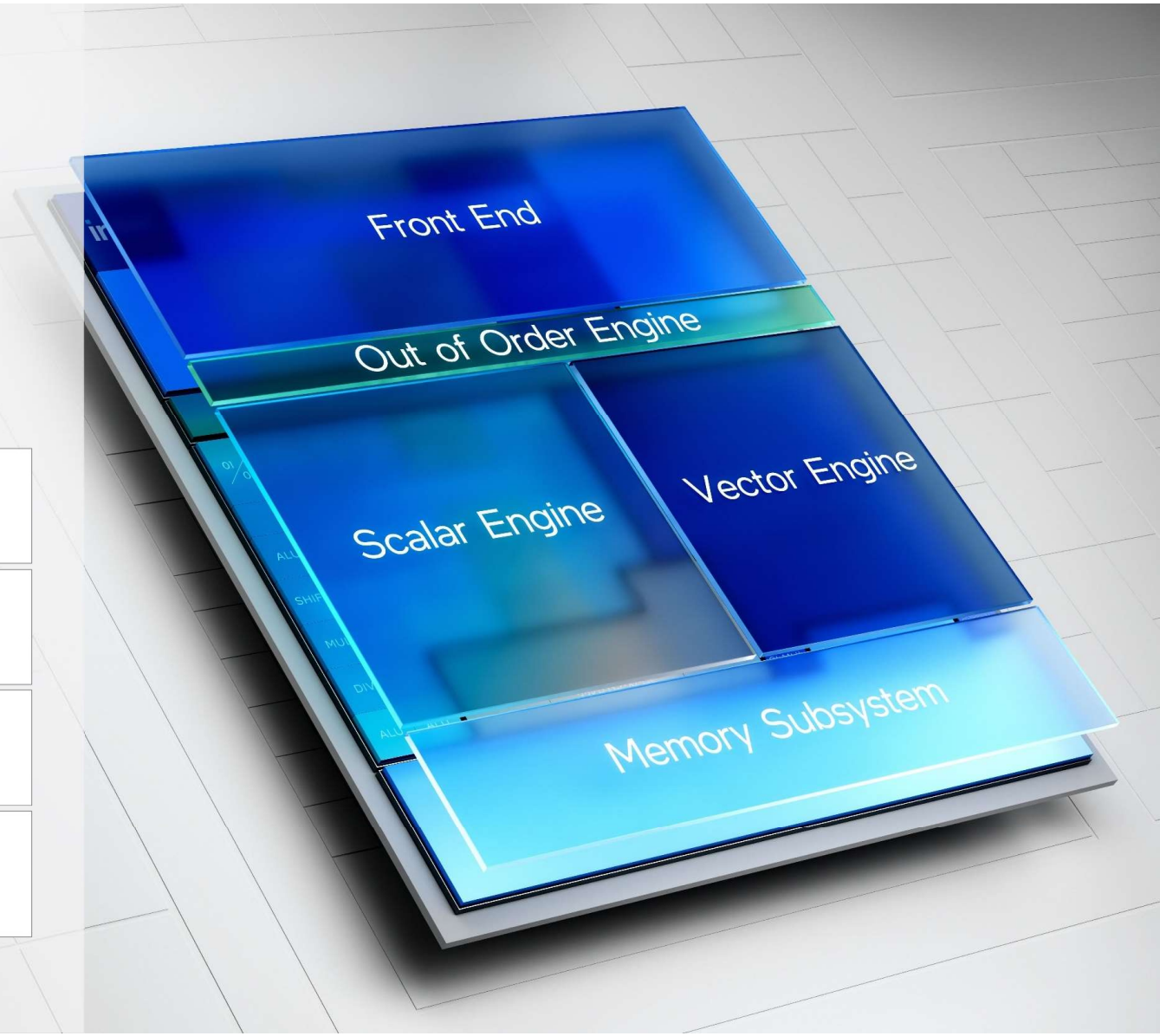
Clearwater Forest E-core

Architectural Leaps forward
for E-core based Xeons

- **Smarter Front-End**
- **Deeper out of Order Engine**
- **Bigger Scalar and Vector Execution**
- **Enhanced memory Subsystem**



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Clearwater Forest E-core

Front-End

64kB Instruction Cache
with on-demand instruction length decoder
accelerating workloads with large code footprints

Nine instructions decoded per cycle
Three 3-wide instruction decoders provide **50% more instruction bandwidth** while keeping power and latency in check

More accurate branch prediction
through deep branch history
and larger structure sizes

Compared to Sierra Forest with E-Core

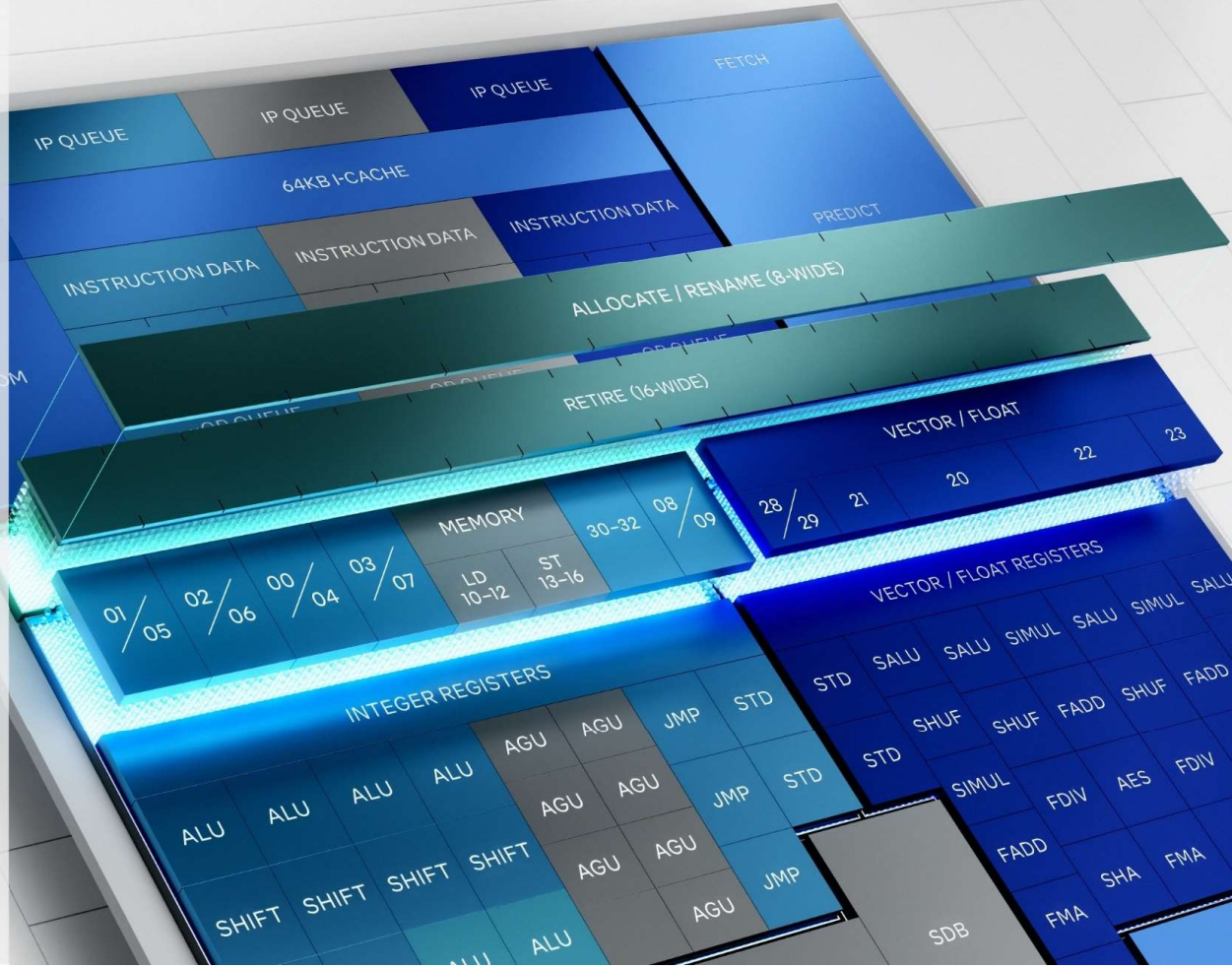
Clearwater Forest E-core

Out-of-Order Engine

Eight-wide allocation (1.6x) with sixteen-wide retire (2x)
Provides execution parallelism

416 entry out of order window (1.6x)
Discovers data parallelism

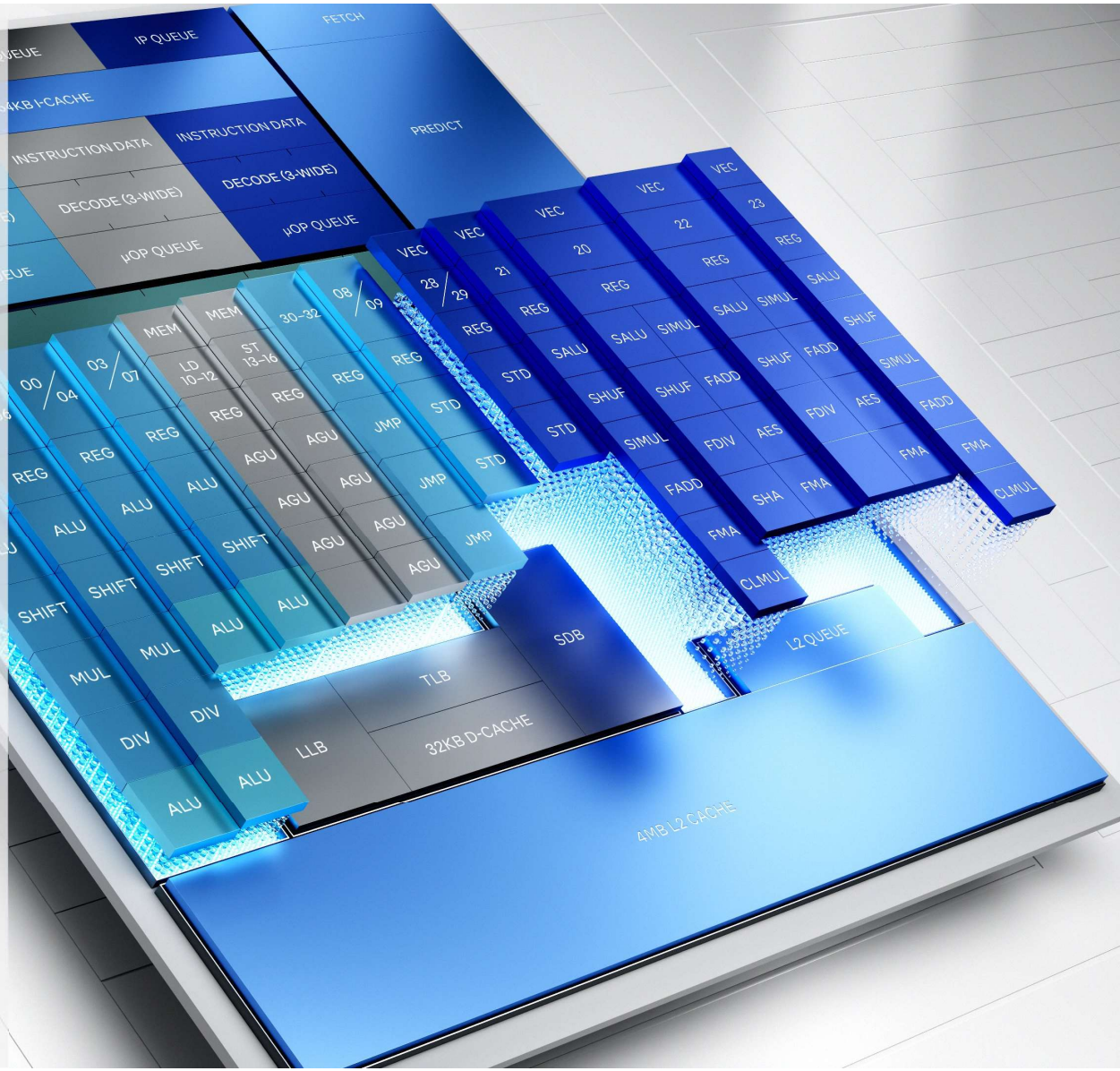
Twenty-six execution ports (1.5x)
Executes data parallelism



Compared to Sierra Forest with E-Core

Clearwater Forest E-core

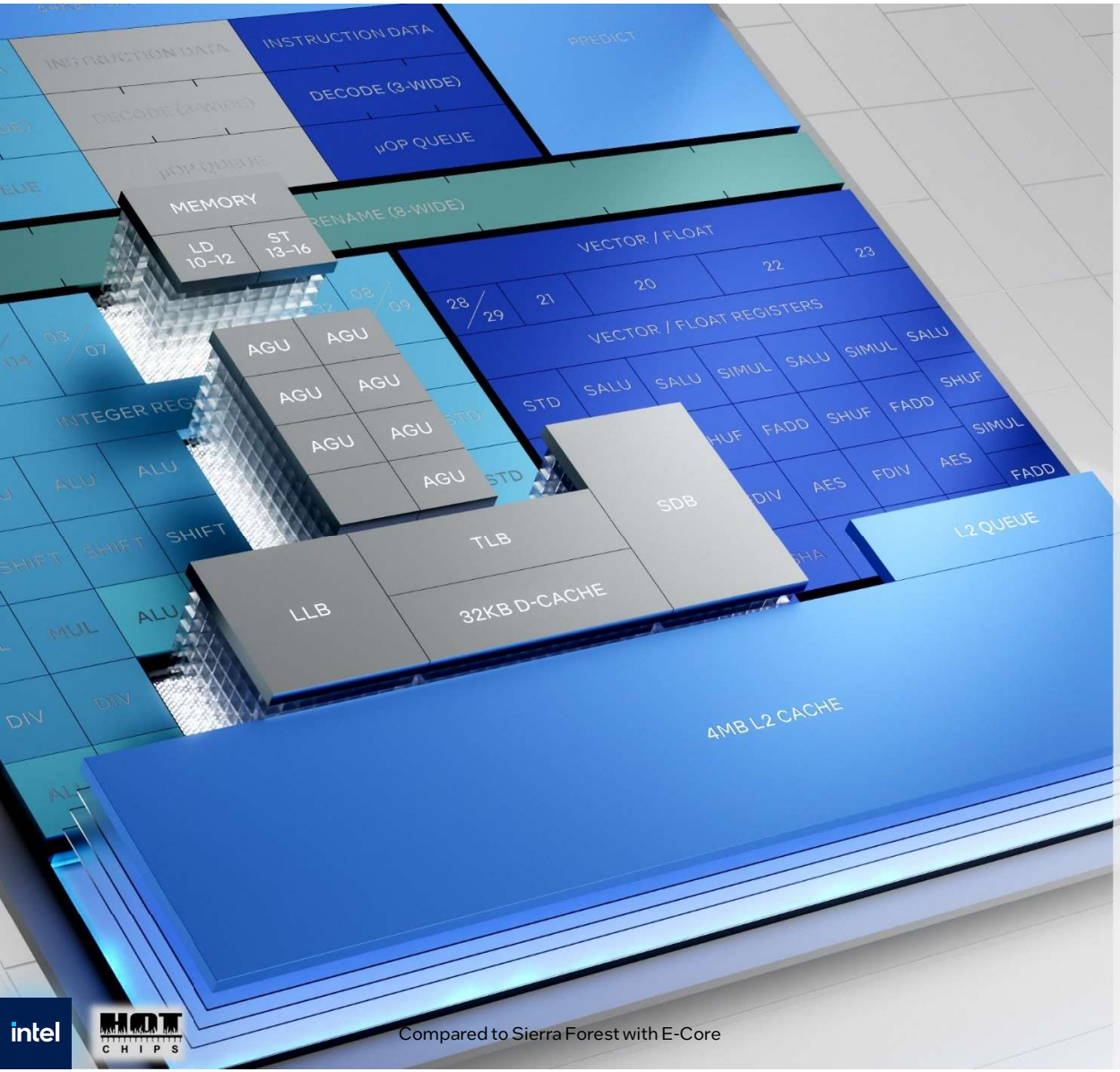
Execution Engine



Twenty-six execution ports
Addresses a breadth of workloads
Dedicated hardware improves efficiency

Integer Execution (2x)
Vector Execution (2x)
Load Address Generation (1.5x)
Store Address Generation (2x)

Compared to Sierra Forest with E-Core



Compared to Sierra Forest with E-Core

Clearwater Forest E-core

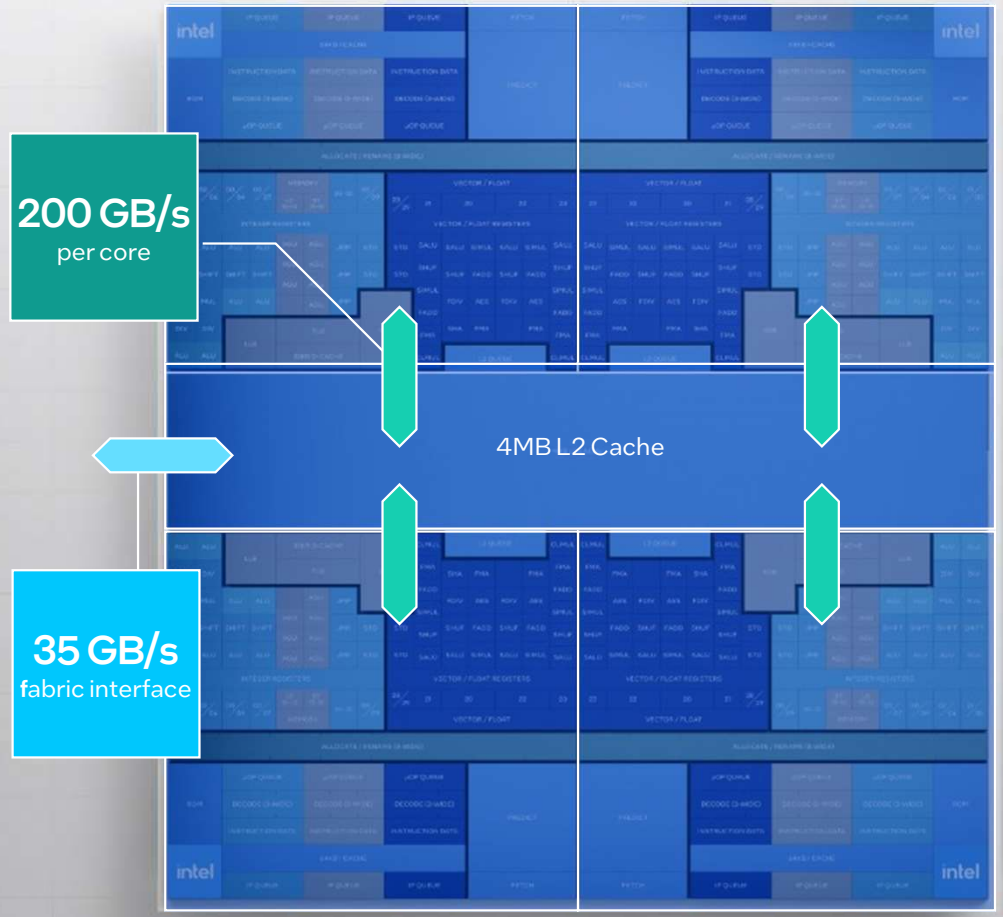
Core Memory Subsystem

Three Load (1.5x) + Two Store (1.0x)
Issuing loads earlier may reduce latency

Deep buffering
Supporting 128 outstanding L2 misses (2x)

Advanced Prefetchers
At all cache levels to detect a wide variety of streams

Xeon® Advanced Features
- L1 Data Cache ECC
- Data Poisoning Support
- Recoverable Machine Check
- Local Machine Check
- 52 physical address bits
- Core Lockstep



Clearwater Forest E-core

Module Architecture

4MB Unified L2
Shared among four cores with 17 cycles of latency

4 Cores per module
Area efficient construction

Twice the L2 Cache Bandwidth
400 GB/s

17% Instructions per cycle increase
SpecIntRate'17 estimated projection

Compared to Sierra Forest with E-Core
Based on architectural projections as of August 2025
Not a physical representation

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3D Construction

Optimize for each process node

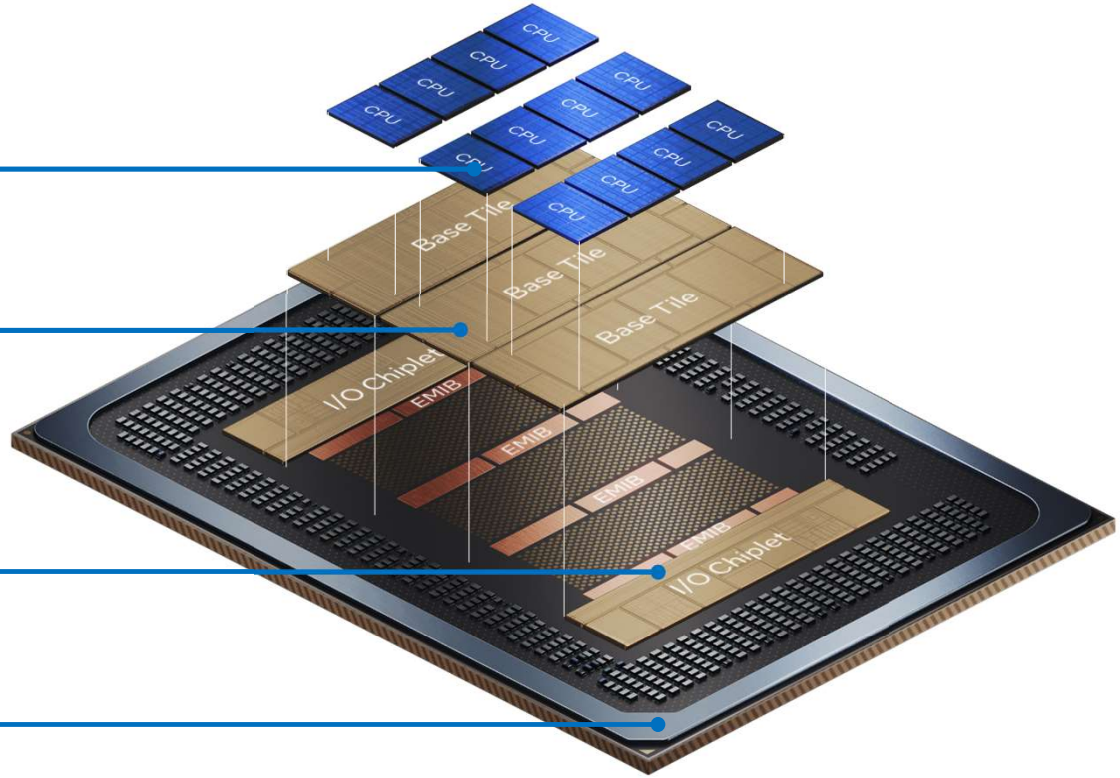
Twelve CPU Chiplets on Intel 18A
E-core modules

Three Base Chiplets on Intel 3
Fabric, LLC, memory controllers and IO

Two I/O Chiplets on Intel 7
High speed I/O, fabric and accelerators

Xeon 69xxE/P Platform Compatible

Monolithic mesh coherent fabric
Power efficiency from shorter routes, more metal resources, high density interconnect



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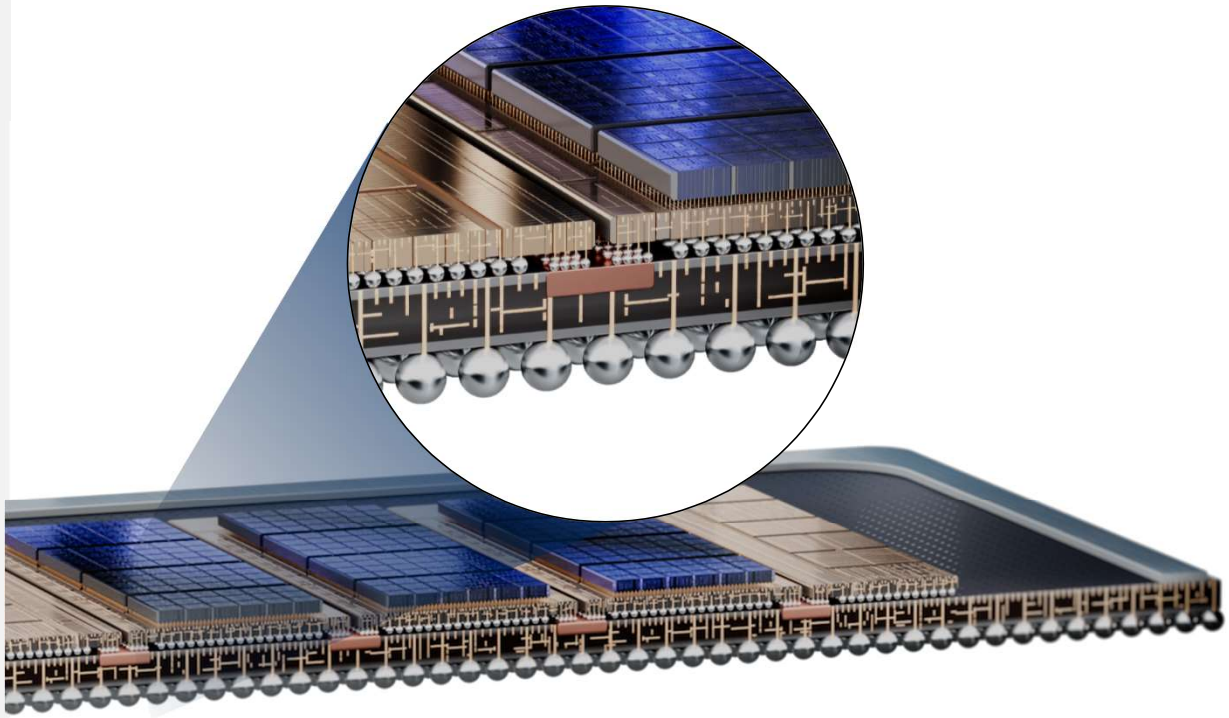

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Performance

2x 12 channels DDR5 8000 Memory bandwidth to support performance increase	**1300 GB/s*** **3 TB**
2x 96 Lanes Gen 5 PCIe, 64 CXL IO bandwidth and connectivity	**1000 GB/s** **96 devices**
144 Lanes UPI Coherency High bandwidth, low latency remote memory access	**576 GB/s**
576 cores, 1152 MB LLC	**59 TF/s** **5000 GB/s**

*2 socket 100% read bandwidth 2R x4
Results are based on architectural projections as of August 2025

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Thank You