Photonic Interconnect for Accelerated Computing

Celestial AI Photonic Fabric Module – The world's first SoC with in-die Optical IO

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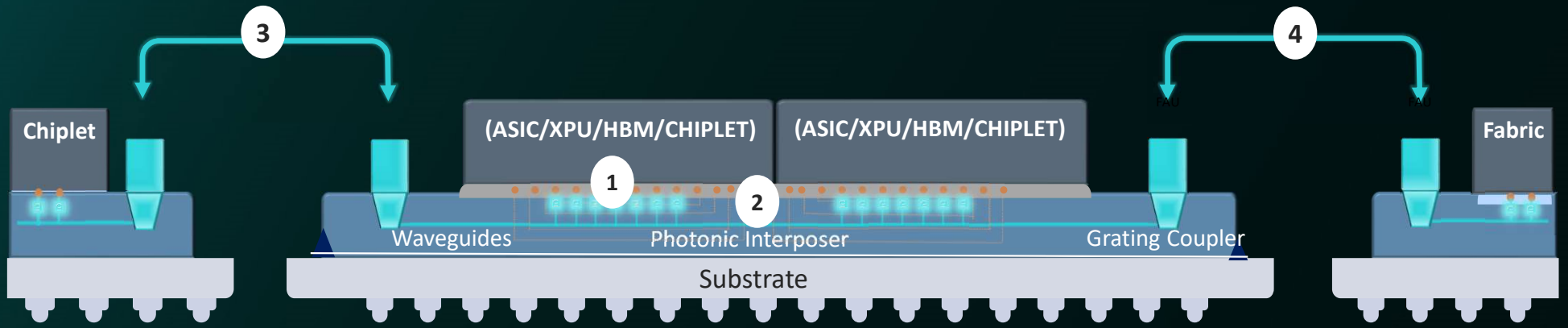
HotChips 2025

Lighting The Path To Exascale AI: Photonics In High Performance Clusters

celestial AI

Celestial AI Photonic Fabric™ Link: PFLink™

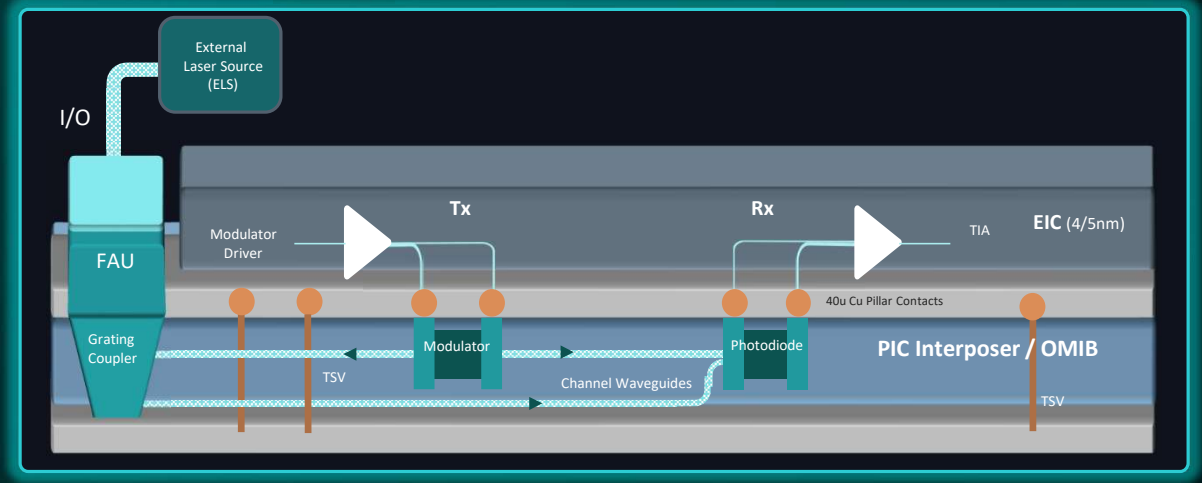


	Photonic I/O	Reach
1	Within Chip	mm
2	Within Package (Die-Die)	mm
3	Package-to-Package	m
4	Package-to-Fabric	m

Photonics integrated directly into a 2.5D interposer using CoWoS

Celestial AI Photonic Fabric™ Link: PFLink™

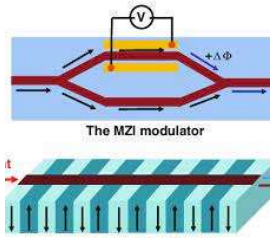
Photonic Fabric™ Link

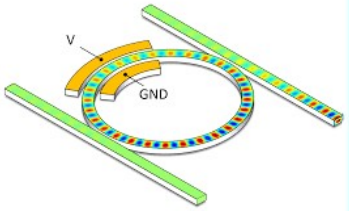


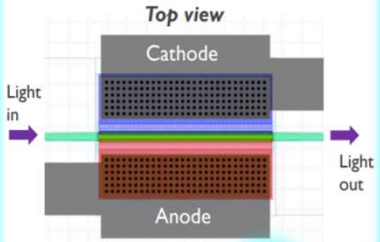
Electronics (EIC) TSMC 4/5nm	**AMS (Analog Mixed Signal) Macro**	Transmitter, Modulator Driver Analog Equalizer Receiver, TIA SerDes - Photonic Optimized
	OMAC Optical MAC	Link Mngt, FEC, Flit Gen, Retransmission, PCS
	NCL	Network Convergence Layer Protocol adaptive
Advanced Packaging		
Photonic Interposer or Bridge		Photonic Integrated Circuit (PIC) FAU (Fiber Array Unit) EAM: Compact Thermally Stable Modulators Photodiodes SiPh Waveguides Grating Coupler

FAU = Fiber Attach Unit

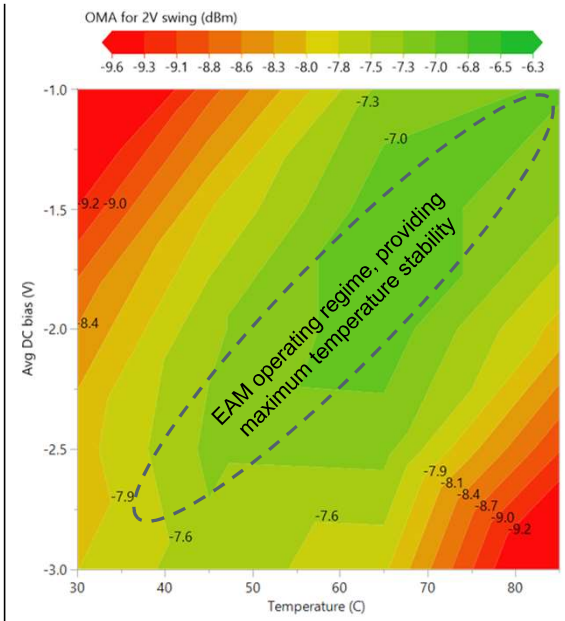
Celestial AI Silicon Photonics Differentiation







Metric	MZI	Ring Modulator	EAM
Size	1000-1200u	<50u	~50u
Thermal Stability	Yes (>50°C)	No (<1°C)	Yes (>50°C)
Speed (Data Rate)	56+Gbps	56+Gbps	56+Gbps
Power	High Power	Low Power	Low Power
Optical Bandwidth	Optically Broadband	Narrow Band (<1nm)	30nm
XPU Integration	Low BW Density	Thermal Incompatibility	Ideal



EAM Thermal Stability
> 85°C range with DC Bias

EAMs: Electro Absorption Modulators
The only solution for Scale-Up Interconnect

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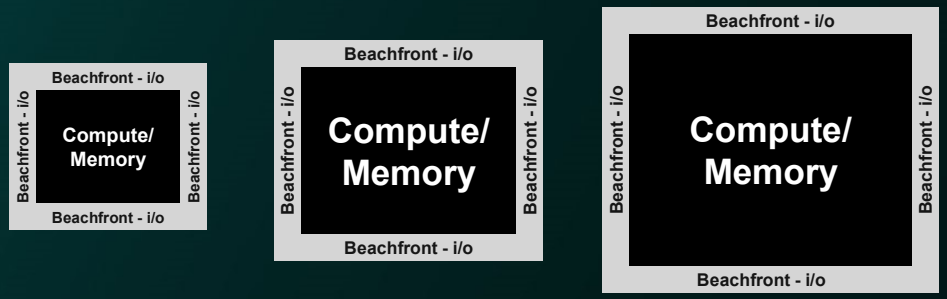
Base Thesis of Celestial AI
Electronic Fabric vs Photonic Fabric Scaling Laws

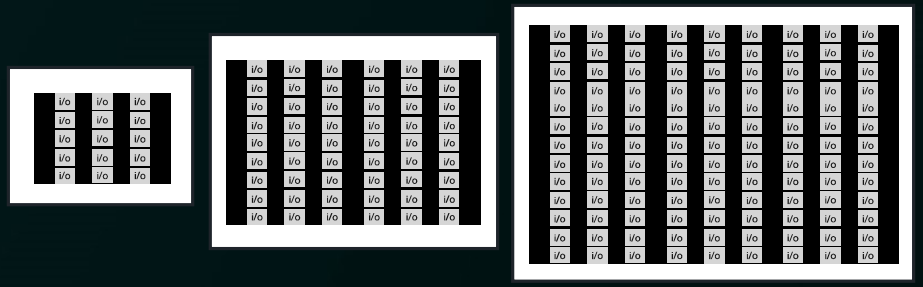
Electronics



Silicon Area

Latency ~ constant + L*__1ns/mm__

Optics



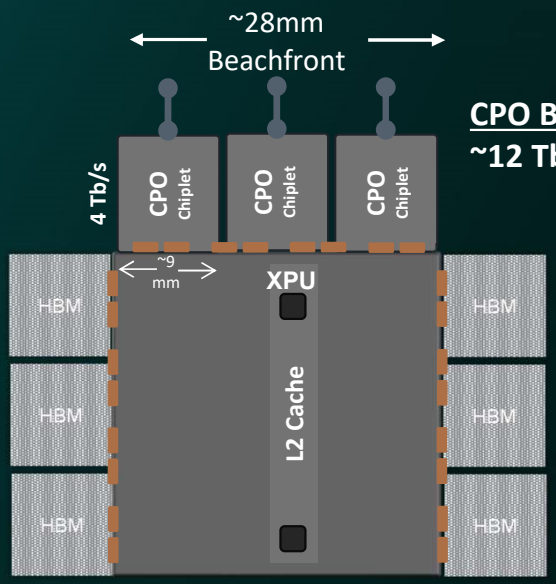
Silicon Area

Latency ~ constant + L*__0.002 ns/mm__,
i.e. approximately constant

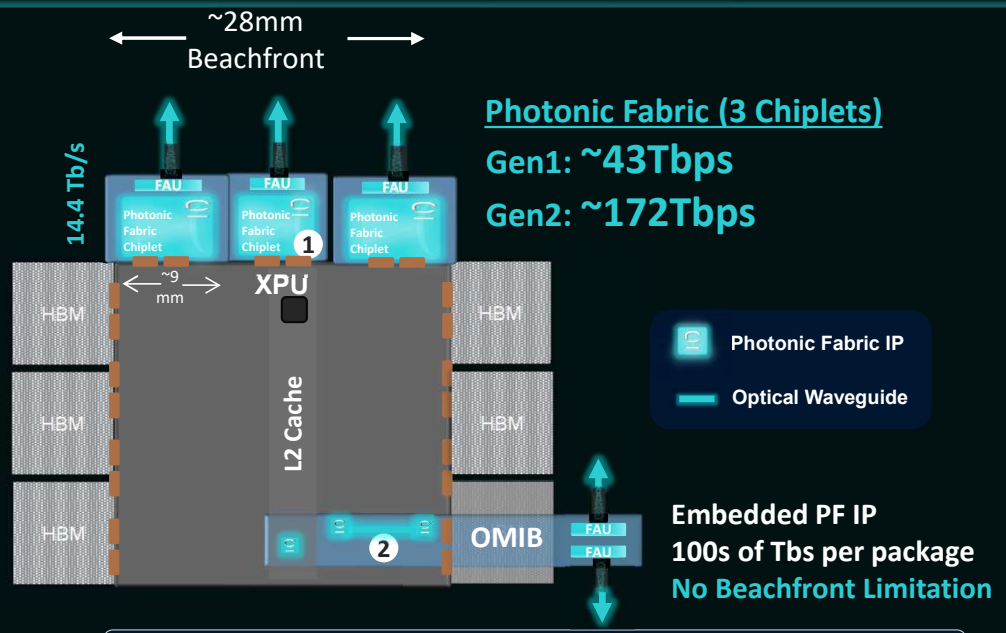
Fabric	Electronics	Optical
Compute/SRAM	$\propto mm^2$	$\propto mm^2$
Bandwidth	mm	$\propto mm^2$
Latency	mm	Constant

Bandwidth (mm^2) scales with compute (mm^2) at constant latency

Photonic Fabric™ Beachfront Advantage



CPO BW (3 Chiplets)
~12 Tb/s



Photonic Fabric (3 Chiplets)
Gen1: ~43Tbps
Gen2: ~172Tbps

Embedded PF IP
100s of Tbs per package
No Beachfront Limitation

Beachfront Limited Bandwidth
- Edge coupling & Advanced packaging limitations

CPO & Electrical PHY
- Electrical PHY & CPO deliver data only to the edge of the die

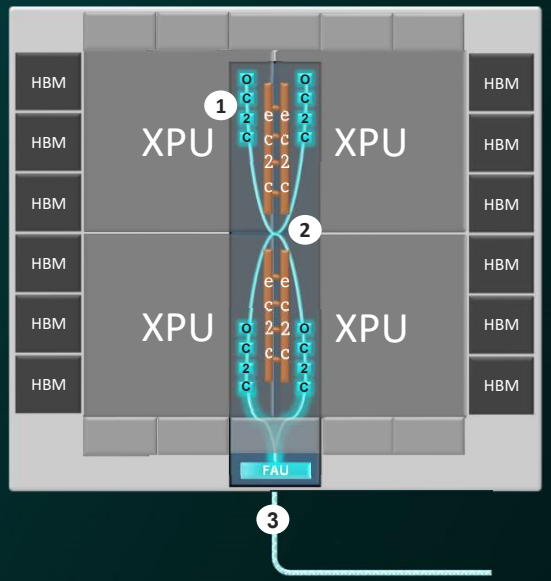
1. **Photonic fabric chiplets**
Beachfront density/mm: Gen1 = ~2Tbps; Gen2 = ~8Tbps

2. **OMIB: Optical MultiChip Interconnect Bridge**
Embedded photonic fabric IP in XPU
Areal density: (1.8Tbps, ~1.8mm²)

Delivers Data at the Highest Bandwidth Densities with no Beachfront Limitation

OMIB: Embedded Photonic Fabric

Optical Multi-Chip Interconnect Bridge (OMIB)



Photonic Fabric IP

O C 2 C Optical Chip-to-Chip

e c 2 c Electrical Chip-to-Chip

OMIB Benefits:

01. Optical Integration in multi-kW package
02. EAM thermally stable modulation
03. XPU die: High-speed I/O
04. NO Beachfront limitations: Available for I/O and Memory
05. Reduces package-to-package I/O latency and power
06. Compatible: CoWoS & glass panel integration
07. Highest package I/O density (80+ fiber FAUs, HVM process)

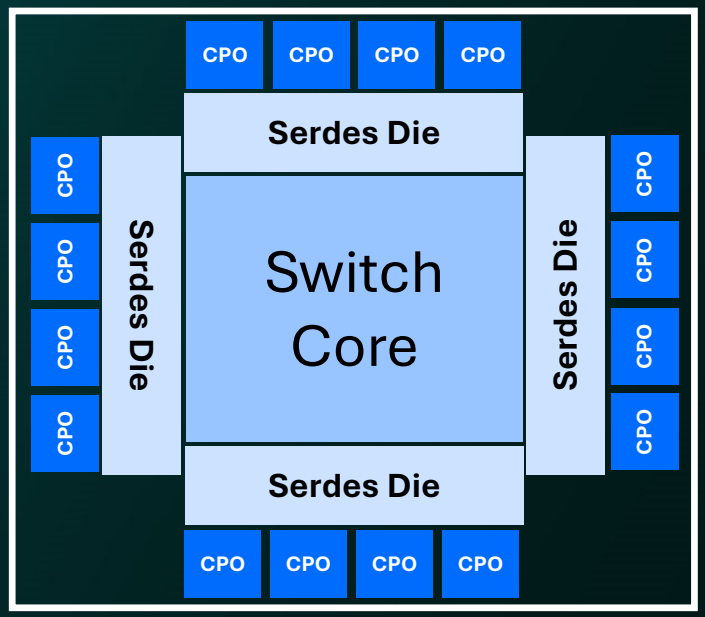
	Photonic I/O	Reach
1	Within Chip	mm
2	Within Package (Die/Chiplet or Die/Die)	mm
3	Package-to-Package	Meters

High Density Photonic Interconnectivity of Multi-Chip Packages

Freeing Up the Beach Front

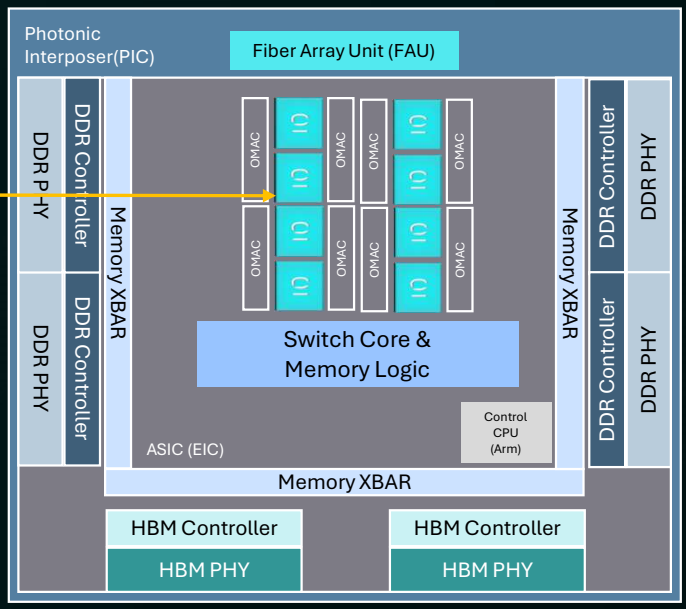
What Will You Do With All The Beachfront?

Conventional CPO



Optical IO in the center of the ASIC

Photonic Fabric Module



Entire Beachfront Consumed by optical IO
No beachfront for memory or other PHY

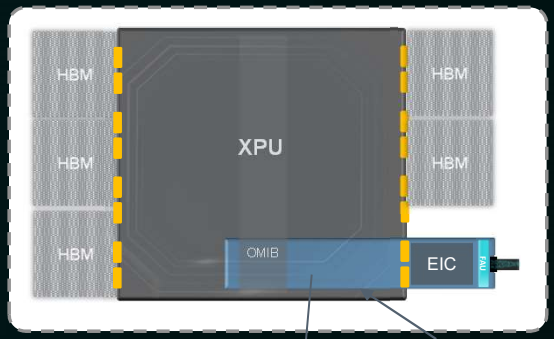
Optical IO in the **center of TSMC 5nm** silicon

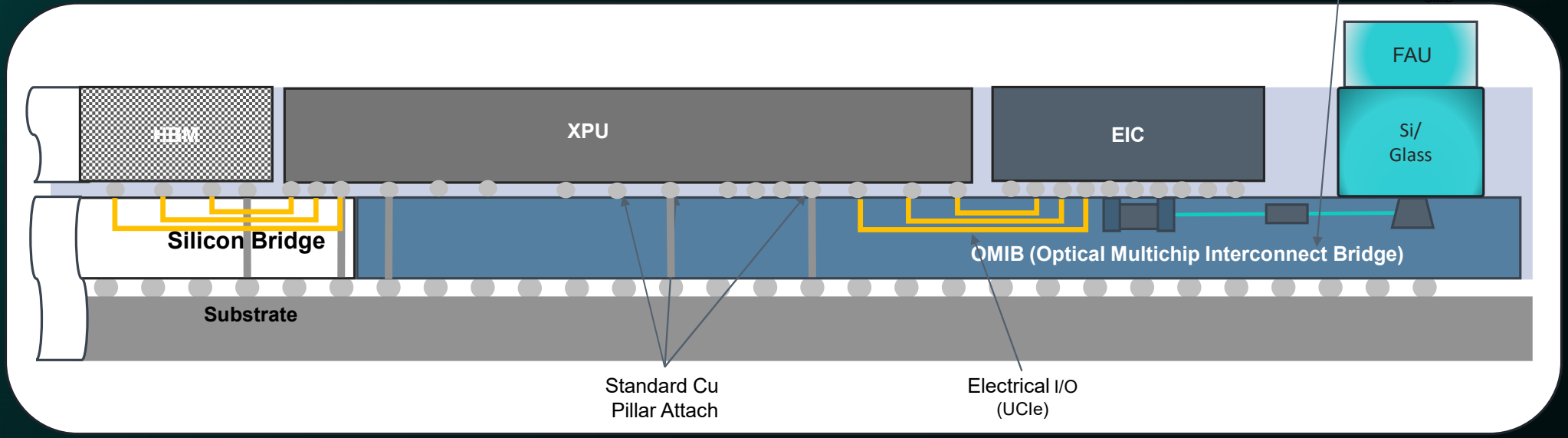
E-W beachfront used for 4x DDR PHY & Controller
S beach-front used for 2x HBM PHY & Controller

Photonic Fabric Chiplet with OMIB (CoWoS®-L)

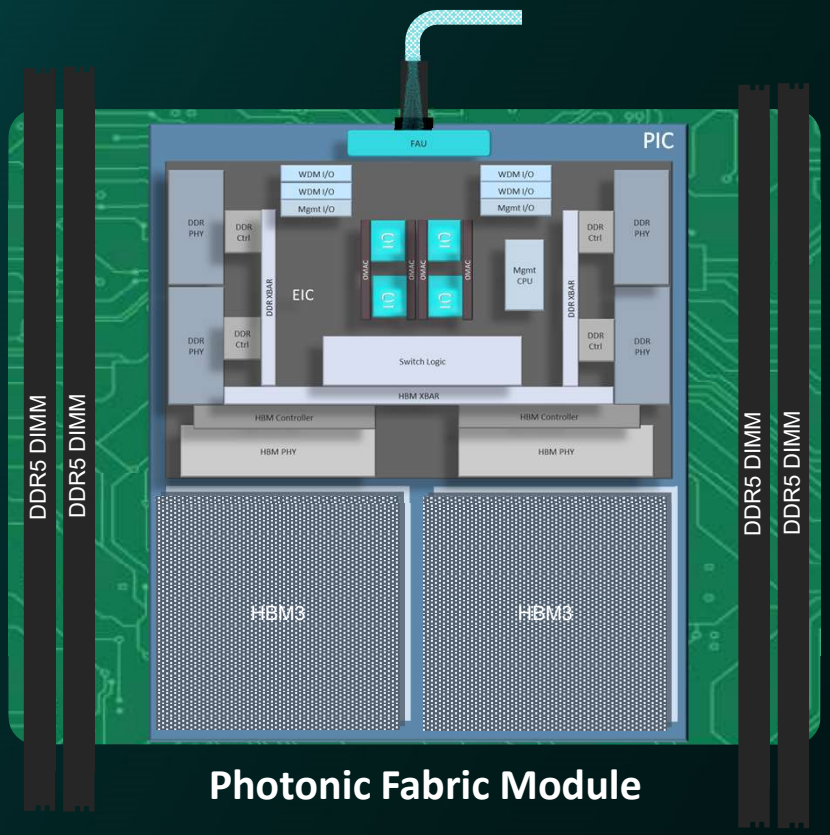
CHIPLET Features

- EIC + OMIB + FAU
- OMIB extends under the XPU for connectivity

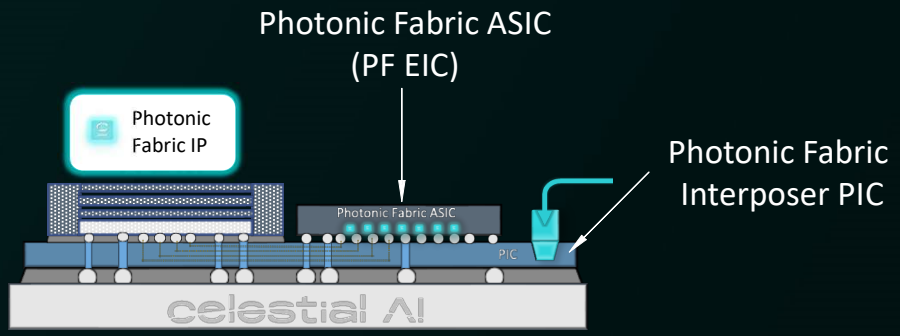




Photonic Fabric™ Module Gen1



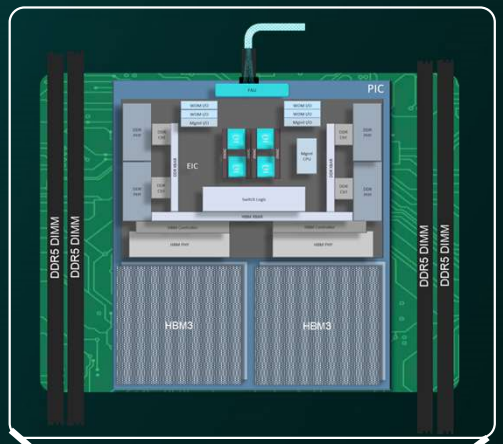
Photonic Fabric Module



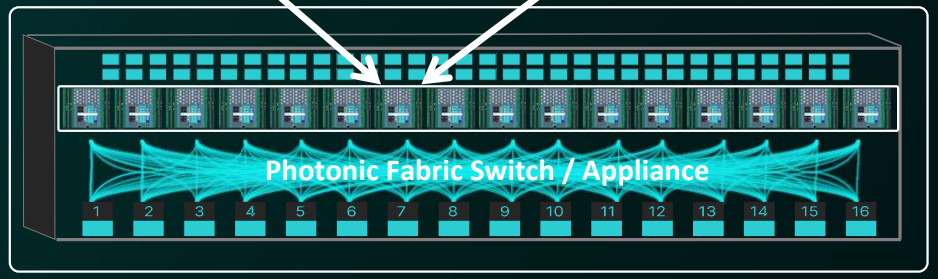
<u>Photonic Fabric Switch/Appliance Gen1</u>:
Integrated switching: Multiheaded device with 256 Channels and 16 concurrent ports

<u>In-Network Shared Memory (Gen1)</u>
HBM Capacity per Module: 48-72 GB
- DDR Capacity per Module: 2TB
- Bandwidth per Module: 7.2Tb/s (full duplex)*
- HBM operates as write-through cache for DDR
- Hardware Semaphores

Photonic Fabric™ Link: Module & Appliance



Side View



Photonic Fabric Module

Celestial AI Designed System in Package (SIP)

- Memory Controllers + Photonic Fabric™ Link + Network Switch

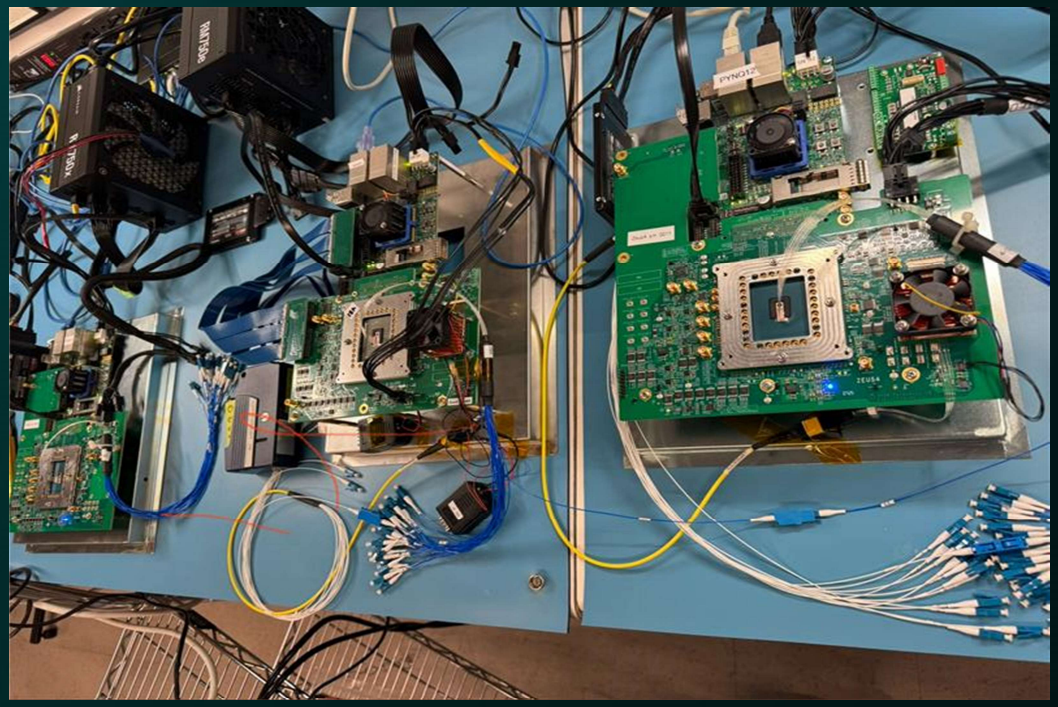
2.07 TB Memory Capacity at 7.2 Tbps Bandwidth with ~ 200ns Latency

- HBM3E Operates as Write-through Cache for DDR
- Bandwidth & Latency of HBM3E with Capacity & Cost of DDR5

Photonic Fabric Appliance

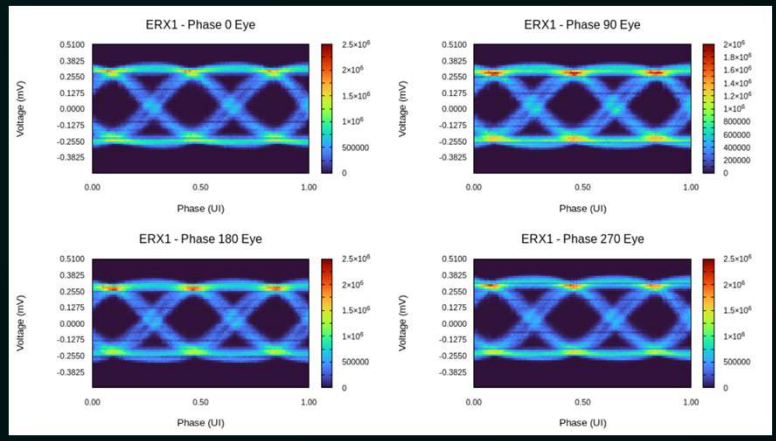
- 16x Photonic Fabric Memory Modules in a 2U Appliance
- 33TB Memory Capacity
- 115Tbps Network Switch Enabling a Scale-Up AI Fabric

Silicon Test Results



Full Link setup with WDM between two test platforms

- TSMC 5/4nm EIC – completed 4 tapeouts
- AMS Quad macro 4 x 4 x 56Gbps NRZ
- Includes PLLs, LDOs, monitor PDs for PIC observation
- Bandwidth density 1.8Tbps in ~1.9mm^2
- Link with WDM shows pre-FEC BER <1e-8
- Power
  - Laser 0.7 pJ/bit
  - Electronics 2.4 pJ/bit



Built-in eye monitor - Rx eye at -10.5dBm OMA

Photonic Fabric™ Module Package